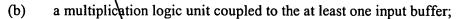
IN THE CLAIMS

Please delete claims 1-23, and add claims 24-41 as follows:

4m /(a)

- A lighting system for graphics processing, comprising:
- at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;
- (b) a multiplication logic unit coupled to the at least one input buffer;
- (c) an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;
- (d) a register unit coupled to the arithmetic logic unit; and
- (e) a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit.
- 25. The system as recited in claim 24, wherein the multiplication logic unit has a feedback loop coupled to an input thereof.
- 26. The system as recited in claim 24, wherein the lighting logic unit is coupled to the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data.
- 27. The system as recited in claim 24, wherein the arithmetic logic unit and the multiplication logic unit include multiplexers.
- 28. The system as recited in claim 24, wherein the multiplication logic unit includes three multipliers coupled in parallel.
- 29. The system as recited in claim 24, wherein the arithmetic logic unit includes three adders coupled in series and parallel.
- 30. A lighting system for graphics processing, comprising:
- (a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;



- (c) an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;
- (d) a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit; and
- (e) memory coupled to the multiplication logic unit and the arithmetic logic unit.
- 31. The system as recited in claim 30, wherein the memory includes a plurality of constants for processing the vertex data.
- 32. The system as recited in claim 30, wherein the memory has a read terminal coupled to the multiplication logic unit.
- 33. The system as recited in claim 30, wherein the memory has a write terminal coupled to the arithmetic logic unit.
- 34. A lighting system for graphics processing, comprising:
- (a) a multiplication logic unit;
- (b) an arithmetic logic unit coupled to the multiplication logic unit;
- (c) a register unit coupled to the arithmetic logic unit;
- (d) a lighting logic unit coupled to the arithmetic logic unit and the multiplication logic unit; and
- (e) memory coupled to the multiplication logic unit and the arithmetic logic unit.
- 35. A lighting system for graphics processing, comprising:
- (a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom; and
- (b) a lighting logic unit adapted for receiving the vertex data;
- (c) wherein the lighting logic unit is capable of setting a flag upon the vertex data satisfying predetermined criteria.
- 36. A method for flagging in a graphics processing module, comprising:
- (a) processing vertex data in a graphics processing module;

- (b) outputting the processed vertex data; and
- (c) setting at least one flag upon the vertex data satisfying predetermined criteria.
- 37. The method as recited in claim 36, wherein the graphics processing module is a lighting module.
- 38. The method as recited in claim 37, wherein a lighting logic unit of the lighting module sets the flag.
- 39. The method as recited in claim 36, and further comprising clamping a value of an attribute of the vertex data based on the setting of the flag.
- 40. A computer program product for flagging in a graphics processing module, comprising:
- (a) computer code for processing vertex data in a graphics processing module;
- (b) computer code for outputting the processed vertex data; and
- (c) computer code for setting a flag upon the vertex data satisfying predetermined criteria.
- 41. A graphics processing system, comprising:
- (a) logic for processing vertex data in a graphics processing module;
- (b) logic for outputting the processed vertex data; and
- (c) logic for setting a flag upon the vertex data satisfying predetermined criteria.